FIG.1

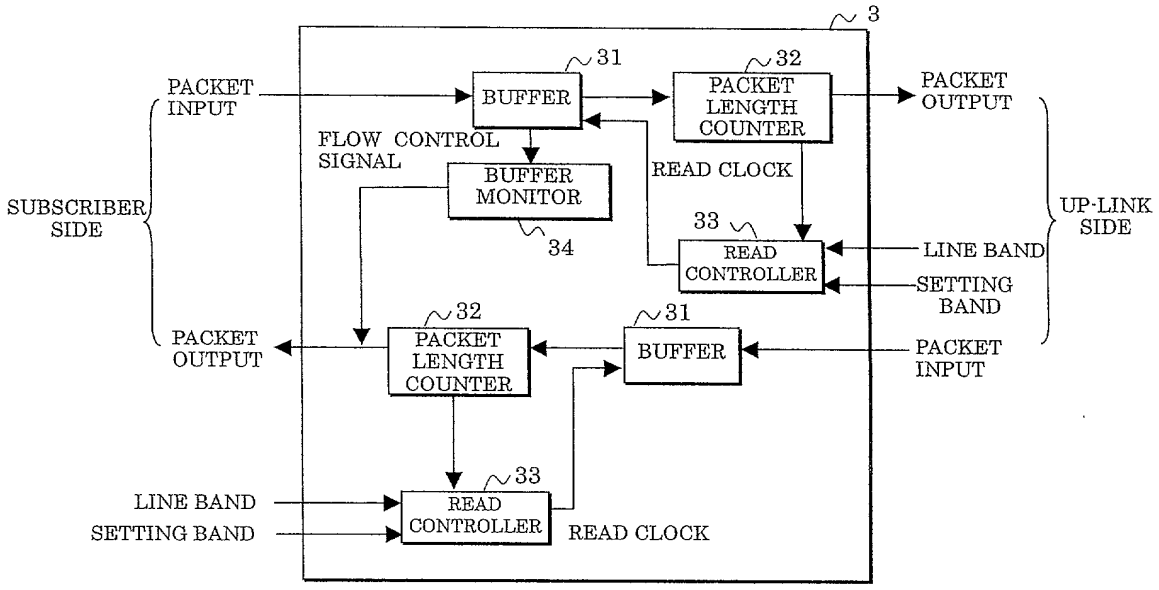
3
31
32
PACKET INPUT
BUFFER
PACKET LENGTH COUNTER
PACKET OUTPUT
FLOW CONTROL SIGNAL
BUFFER MONITOR
READ CLOCK
SUBSCRIBER SIDE
34
33
READ CONTROLLER
LINE BAND
SETTING BAND
UP-LINK SIDE
32
31
PACKET OUTPUT
PACKET LENGTH COUNTER
BUFFER
PACKET INPUT
33
LINE BAND
READ CONTROLLER
SETTING BAND
READ CLOCK

FIG.2

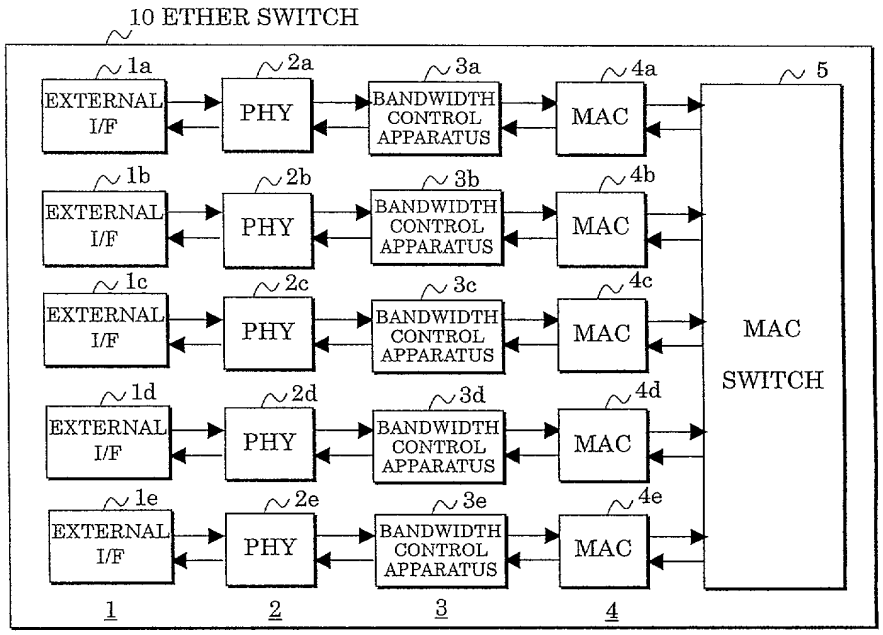
10 ETHER SWITCH
1a
2a
3a
4a
5
EXTERNAL I/F
PHY
BANDWIDTH CONTROL APPARATUS
MAC
1b
2b
3b
4b
1c
2c
3c
4c
MAC SWITCH
1d
2d
3d
4d
1e
2e
3e
4e
1
2
3
4

FIG.3

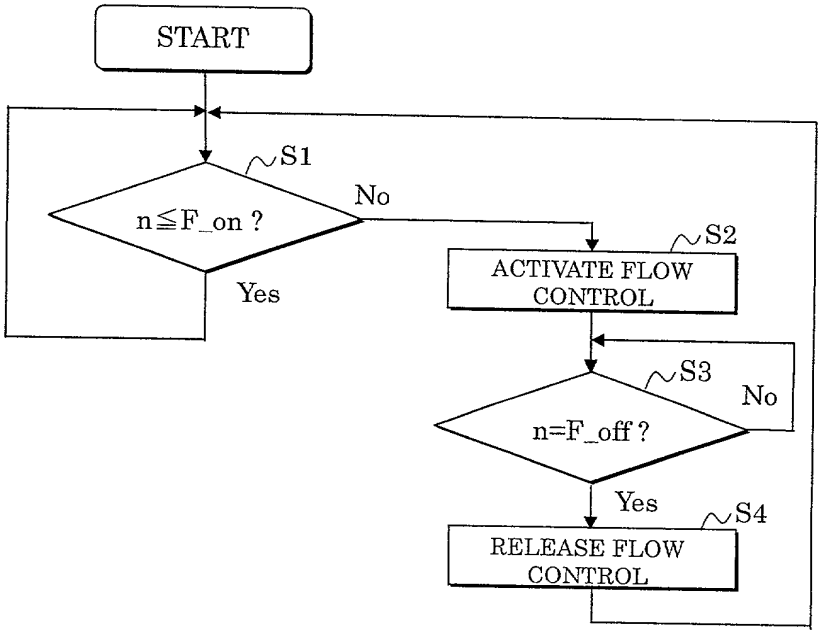
START
S1
n≦F_on ?
No
Yes
S2
ACTIVATE FLOW CONTROL
S3
n=F_off ?
No
Yes
S4
RELEASE FLOW CONTROL

FIG.4

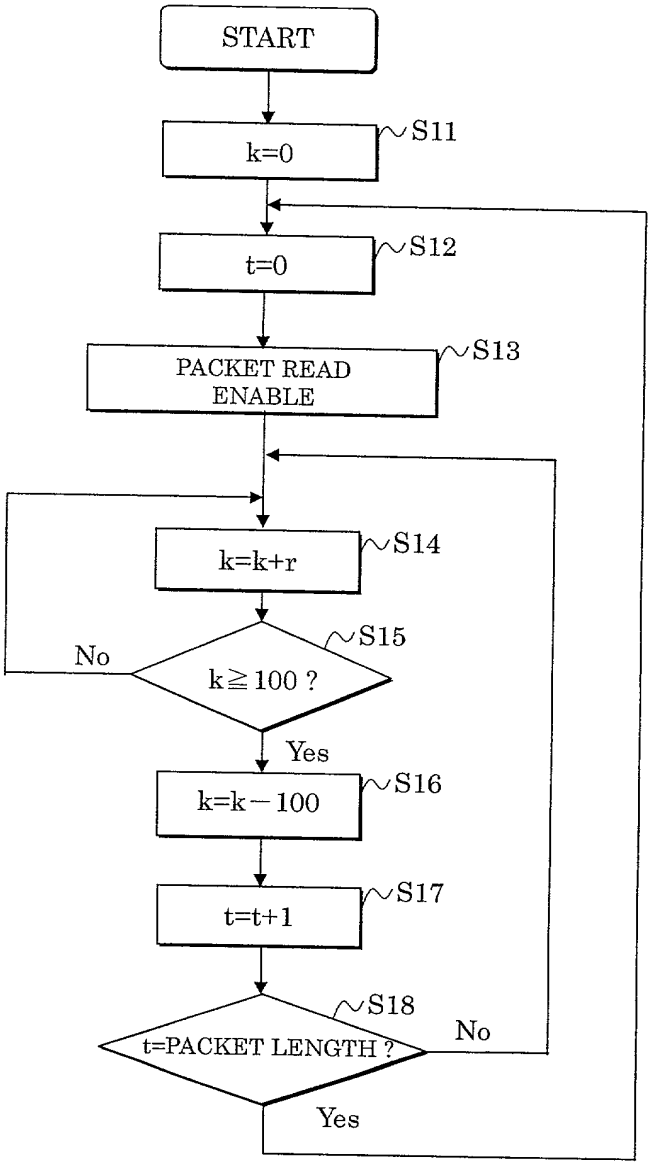
START
k=0
S11
t=0
S12
PACKET READ ENABLE
S13
k=k+r
S14
k≧100 ?
S15
No
Yes
k=k−100
S16
t=t+1
S17
t=PACKET LENGTH ?
S18
No
Yes

FIG.5

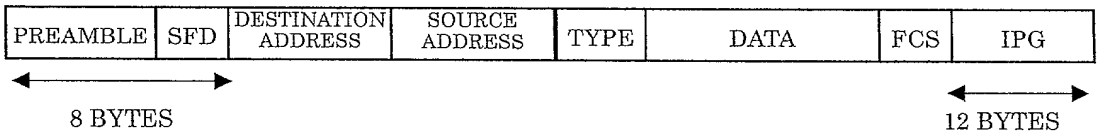

FIG.6A 50 Mbps

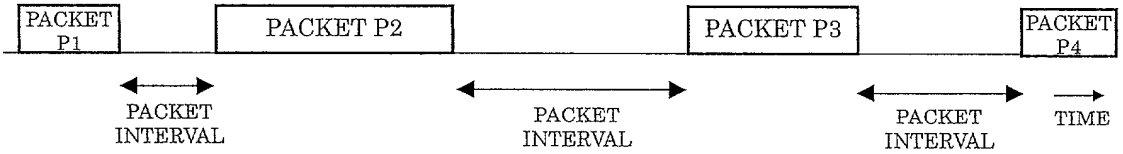

FIG.6B 10 Mbps

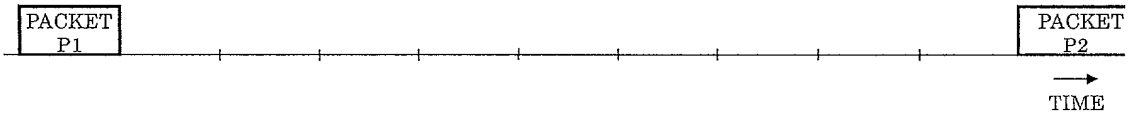

FIG.6C 99 Mbps

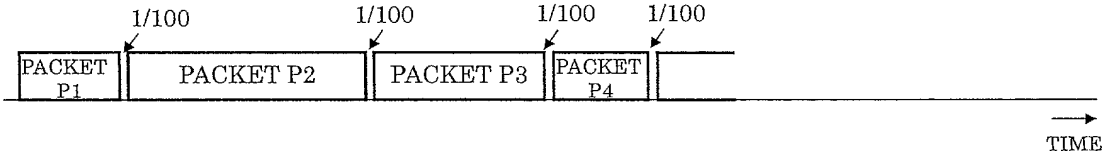

FIG.6D 100 Mbps

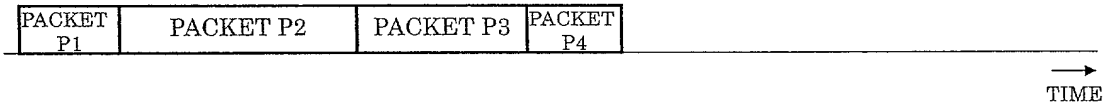

FIG.7A

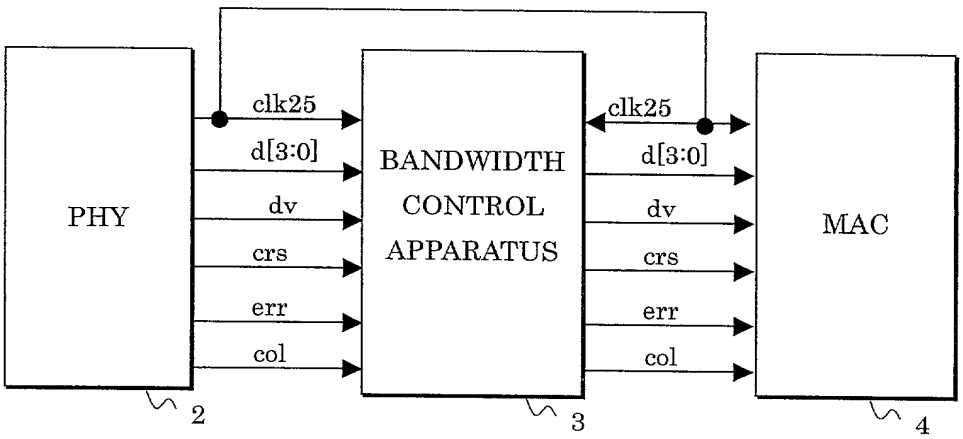

FIG.7B

MII INTERFACE

SIGNAL NAME	INPUT/ OUTPUT	EXPLANATION
clk25	i	CLOCK (25MHz)
d[3:0]	i	DATA
dv	i	DATA VALID (ENABLE)
crs	i	CARRIER SENSE (ONLY RX)
err	i	DATA ERROR (ONLY RX)
col	i	COLLISION DETECTION (ONLY RX.UNUSED)